PROGRAMMABLE PACKET PROCESSOR WITH FLOW RESOLUTION LOGIC

ABSTRACT

A programmable packet switching controller has a packet buffer, a pattern match module, a programmable packet classification engine and an application engine. The packet buffer stores inbound packets, and includes a header data extractor to extract header data from the inbound packets and to store the extracted header data in a header data cache. The header data extractor also generates a header data cache index and provides it to the packet classification engine for it to retrieve the extracted header data. The packet classification engine has a decision tree-based classification logic for classifying a packet. Each of the leaves of the tree represents a packet classification. The packet classification engine uses the header data cache index to retrieve the header data to perform multiple header checks, starting at a root of the tree and traversing branches until a leaf has been reached. The application engine has a number of programmable sub-engines arrayed in a pipelined architecture. The packet classification engine provides start indicators based on the packet classification to the programmable sub-engines to identify application programs to be executed. The sub-engines includes a source lookup engine, a destination lookup engine and a disposition engine, which are used to make a disposition decision for the inbound packets in a processing pipeline. The pattern match module is used to compare the packet to a pre-defined pattern in order to provide a disposition recommendation.